PerfectVIPs
Right Tools... Perfect Chip

USB ATTACHED SCSI VIP

DATASHEET
Rev. 2b

GENIE-UAS

USB ATTACHED SCSI VERIFICATION IP

OVERVIEW

The Genie-UAS UAS Verification IP Products are the industry's most advanced verification solution for UAS designs. The intelligent **Verification Engine** provides a full timing based bus functional model (BFM) for automatic constrained-random stimulus generation and protocol checking. It has a powerful Error Injector and extensive list of callbacks. A unique **Interface Inspector** provides the monitoring, checking, and scoreboarding capability along with protocol compliance, functional coverage and error reporting. A comprehensive **Compliance Suite** is available with test cases for complete verification including corner cases which relieves engineers from the need to manually write tasks. This provides the Perfect combination of tools to ensure design success.

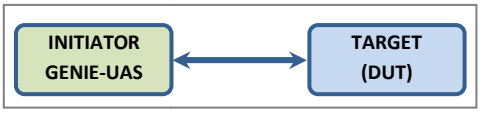

Fig. 1: Example Target Design Verification

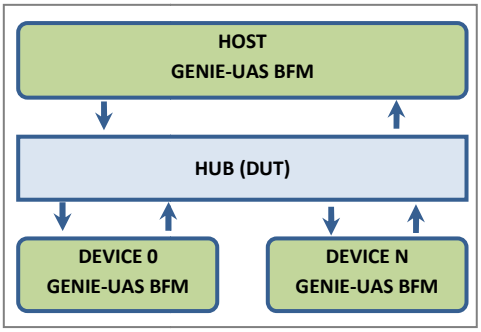

Fig. 2: Example Hub Design Verification

The **Genie-UAS VIP** provides a quick and efficient way to verify any UAS and USB 3.0 based design – Host, Device, Hub or PHY. It supports the UAS 2.0, UASP 1.0 and USB 3.0 specification and tests UAS and all layer levels of the USB 3.0 design – PHY, Link and Protocol. Genie-UAS provides a complete verification solution that includes multi-language support and UVM and OVM methodology.

The Genie-UAS VIP provides:

- Bus Functional Models
- Protocol Checker
- Protocol Monitor
- Scoreboard
- Report Generator
- Error Injector
- Extensive Functional Coverage
- Callback Capability

FEATURES

❖ Compliant to UAS 2.0, UASP 1.0, USB 3.0 and USB PIPE 1.0 specification	❖ Configurable for 0 to n endpoints
❖ Supports SAM-4, SPC-3 and SBC-3 SCSI packets	❖ System level and block level testing
❖ Multiple endpoint support	❖ Comprehensive Compliance Suite
❖ Automatic handling of Protocol, Link and PHY layer packets	❖ Automatic /user configurable generation of flow control packets
❖ Supports out of order transaction and queuing	❖ Multiple Language Interface – SystemVerilog and Verilog
❖ Complete Functional USB 3.0 Verification - Host, Device, Hub & PHY	❖ Configurable TS1, TS2, TSEQ, SKP ordered set generation
❖ Full Link Training & Status State Machines (LTSSM)	❖ Configurable packet size for data packet payloads
❖ Supports Power Management : i. Low power mode enable/disable (U1/U2) ii. Suspend (U3) iii. Active state (U0) iv. Resume/Remote Wakeup	❖ Hub configuration support: i. Packet generation directed for Hubs ii. LMP packet generation iii. Data transactions to device connected to Hub iv. Generation/storing of Hub specific descriptors v. Control transactions specific to Hub
❖ Automatic /user configurable generation of all LMP packets	❖ Supports randomization for all BFM Knobs and error injections
❖ Automatic /user configurable generation of isochronous time stamp packets (host configuration)	❖ Supports all USB transactions: Control, Isochronous, Interrupt, Bulk and Bulk Streaming
❖ Supports LFPS signal generation and detection	❖ Supports UVM and OVM
❖ Support for generation of all link commands	❖ Easily integratable into any environment

VMMenabled UVM OVM

PRODUCT DETAILS

UAS Initiator

The Genie-UAS Initiator VIP provides a full timing, bus functional model (BFM) that operates at 5 Gbps, SuperSpeed rates. The BFM initiates SCSI commands and emulates the interface. The programmable Error Injector permits errors to be inserted at any layer of the protocol.

- Multiple endpoint support for multiple UAS PIPE
- Initiator performs bus enumeration and allocates independent UAS pipes for communication flow
- Generates user configurable SCSI Command IU for data-in, data-out and simultaneous data transfer
- Generates Task Management IU to request task management function

UAS Target

Like the Genie-UAS Initiator, the Genie-UAS Target supports all the features and functions of the UAS and USB 3.0 device specification.

Multiple endpoint support for multiple UAS PIPE

- Supports out of order transaction and queuing
- Generates User configurable Sense IU and Response IU
- Supports automatic generation of Write Ready IU and Read Ready IU

USB PHY

Integrated into the Initiator and Target BFM, the USB PHY model provides accurate modelling at the serial or PIPE interface.

- Connect to RTL (MAC) on PIPE and PHY on serial side
- Clock and data recovery (SERDES)

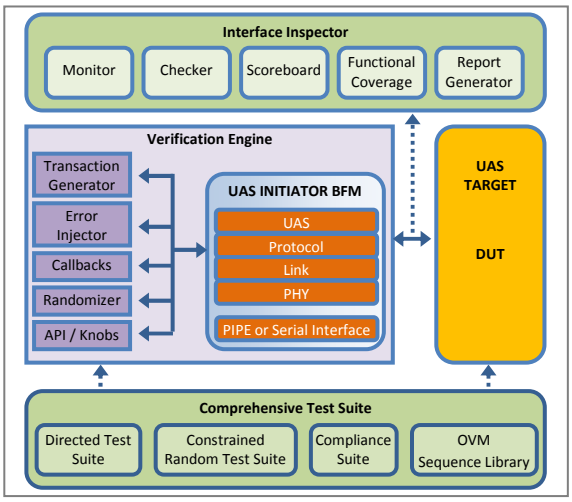

Fig. 3: UAS Target DUT

- 8b/10b encoder/decoder
- Elasticity buffer
- Serial transmission/reception at 5 GHz

UAS Interface Inspector

An enhanced protocol checker and monitor with built in coverage features; it can be integrated into any UAS verification environment, between upstream and downstream ports.

- Checks for protocol compliance and flags violations
- Generates bus performance summary and transaction statistics
- Performs functional/feature/error/protocol compliance coverage

BENEFITS

- ❖ Guarantees compliance to UAS and USB 3.0 specifications
- ❖ Plug-and-play into all major simulation environments
- ❖ Reduces risk to design flaws
- ❖ Enable faster testbench development and complete UAS design verification
- ❖ Ensure first pass design success
- ❖ Reduces overall design and verification costs

UAS COMPLIANCE SUITE

Developed by PerfectVIPs to thoroughly exercise UAS and USB 3.0 designs, the compliance suite is an advanced verification test suite that provides hundreds of test cases.

- Verifies UAS and all layers of USB 3.0 designs
- Provides comprehensive design coverage targeted at UAS, Protocol, Link & PHY layers
- Unified customizable message formatting and reporting
- Inject error at all layers
- Pre-built cover groups for functional coverage analysis
- Powerful and flexible pre-built OVM sequence libraries for generating test scenarios for coverage driven verification
- Pre-built constraint library which allows constrained random stimulus generation ensuring robust verification
- Developed with actual customer designs

UAS SOLUTIONS

Developed by PerfectVIPs to address all USB 3.0 architectures, the following USB 3.0 SuperSpeed solutions are available.

Verification IP:

- UAS Initiator VIP
- UAS Target VIP
- UAS Interface Inspector
- UAS 3.0/2.0 Host VIP
- UAS 3.0/2.0 Device VIP

Compliance Suites:

- UAS Initiator Compliance Test Suite
- UAS Target Compliance Test Suite
- USB 3.0 Host Compliance Test Suite
- USB 3.0 Device Compliance Test Suite
- USB 3.0 Hub Compliance Test Suite

Supported Simulators

- Aldec, Cadence, Mentor and Synopsys

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